EXHIBIT 9

[redacted]

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	Civil Action No. 1:13-cv-01835-RGA

EXPERT REPORT OF DR. TODOR COOKLEV, Ph.D., REGARDING INFRINGEMENT OF THE FAMILY 3 PATENTS

[redacted]

More precisely byte B_j (with index j) shall be delayed by $\Delta[j] = (D - 1) \times j$ bytes, where D is the interleaver depth in bytes, and D and I are co-prime (have no common divisor except for 1).").

62. For a VDSL2 transceiver, the interleaver block length "I" may be equal to the number of bytes in a codeword, or may be equal to a fraction of the number of bytes in a codeword (for example, a codeword may be broken up into an integer number of blocks).

C. Interleaver and Deinterleaver Memory

63. The amount of interleaver memory required for a convolutional interleaver can be determined from the block length I and depth D. The illustration of the convolutional interleaver above includes a block length of 5 and a depth of 3 (i.e., $I = 5$ and $D = 3$).

64. As mentioned above, interleaver memory is required because bytes must be stored in order to rearrange the sequence in which the bytes are output. For example, as illustrated above, the last byte (byte #5) of the blue block is delayed by eight byte locations from where it would have been output but for interleaving and, thus, byte #5 would have to be stored during the delay.

65. The combined delay due to interleaving at the transmitter and deinterleaving at the far end receiver (i.e., end-to-end delay) is also function of I and

D. "The end-to-end delay in octets for the interleaver and de-interleaver pair on path *p*, with *p* = 0, 1, is given by:

$$delay\_octet_{x,p} = \left(I_{x,p} - 1\right) \times \left(D_{x,p} - 1\right)$$

where the direction of transmission *x* is either "DS" for the downstream channel or "US" for upstream, $I_{x,p}$ is the interleaver block length, and $D_{x,p}$ is the interleaver depth." TQD114647 (G.993.2 (12/2011)) at p. 25.

66. The amount of interleaver memory required in a transceiver for one latency path is equal to: $delay\_octet_{x,p}/2 = \frac{(I_{x,p}-1)\times(D_{x,p}-1)}{2}$. *See id.* Similarly, the amount of deinterleaver memory required in a transceiver for one latency path is equal to: $delay\_octet_{x,p}/2 = \frac{(I_{x,p}-1)\times(D_{x,p}-1)}{2}$ octets (i.e., bytes) of memory. *See id.*

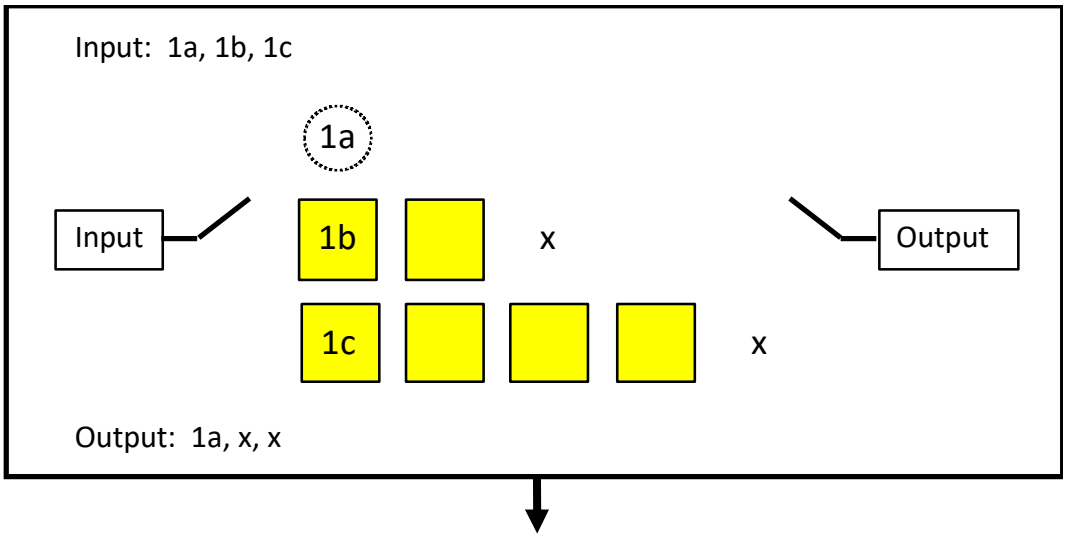
67. For a CPE transceiver implementing one upstream path (US, 0) using interleaving and one downstream path (DS, 0) using deinterleaving, the aggregate interleaver and deinterleaver delay is the sum of $delay\_octet_{US,0}$ and $delay\_octet_{DS,0}$. *See id.* Thus, the aggregate amount of interleaver memory and deinterleaver memory required for the CPE to implement one upstream path (US,0) using interleaving and one downstream path (DS, 0) using deinterleaving is the sum of $delay\_octet_{US,0}/2$ and $delay\_octet_{DS,0}/2$, which is equal to:

$$\frac{\left(I_{US,0} - 1\right) \times \left(D_{US,0} - 1\right)}{2} + \frac{\left(I_{DS,0} - 1\right) \times \left(D_{DS,0} - 1\right)}{2}$$

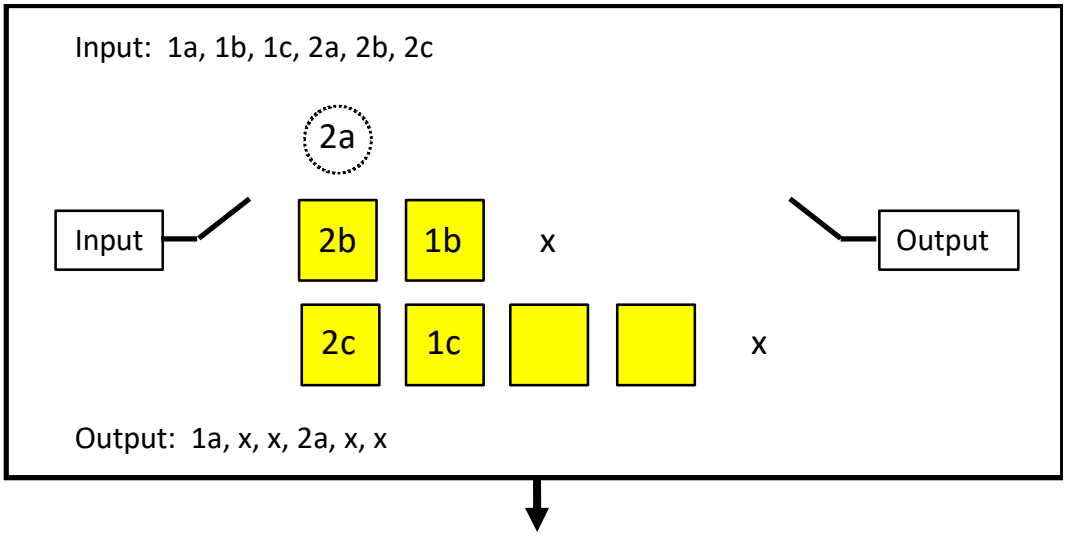
octets (i.e., bytes) of memory. *See id.*

68. The following sequence of figures illustrates a convolutional interleaver (sometimes referred to as a triangular interleaver) with an interleaver block size $I = 3$ and an interleaver depth $D = 7$. This requires $\frac{(I-1)\times(D-1)}{2} = \frac{(3-1)\times(7-1)}{2} = 6$ octets (i.e., bytes) of interleaver memory. The six yellow highlighted square boxes represent the 6 bytes of interleaver memory. The bytes of the first input block are numbered 1a, 1b, and 1c, the bytes of the second input block are numbered 2a, 2b, and 2c, and so on. The dotted circle identifies an output of the interleaver.

69. With reference to the first figure in the sequence below, input byte 1a is immediately output without having to be stored in the interleaver memory, then input byte 1b is stored in the interleaver memory, and then input byte 1c is stored in the interleaver memory. If the interleaver was just initialized, each "x" represents a null output. Or, if the interleaver has already been running, each "x" represents a byte from an earlier-input block.

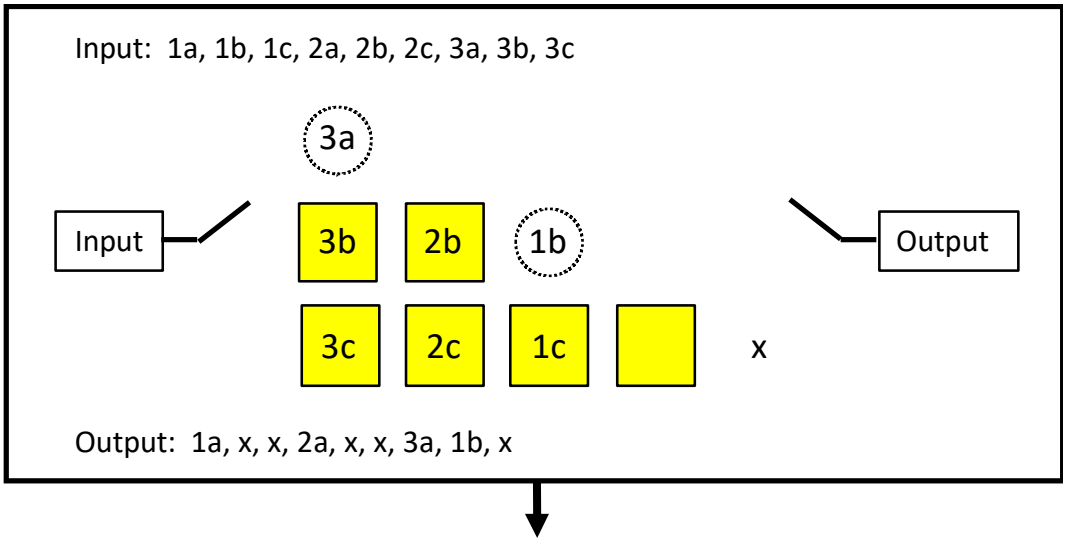


70. With reference to the second figure in the sequence below, input byte 2a is immediately output, then input byte 2b is stored in the interleaver memory, and then input byte 2c is stored in the interleaver memory.

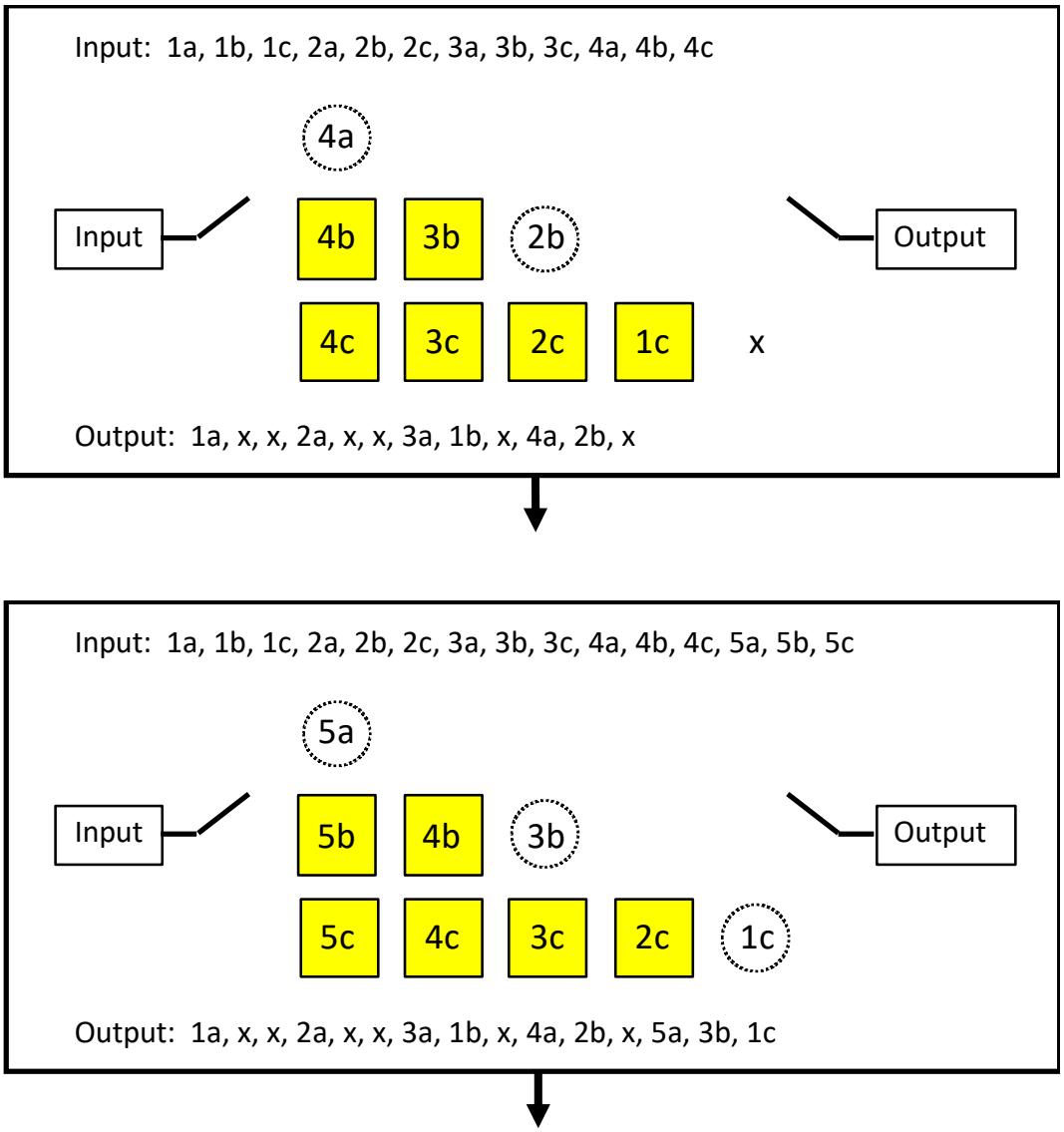


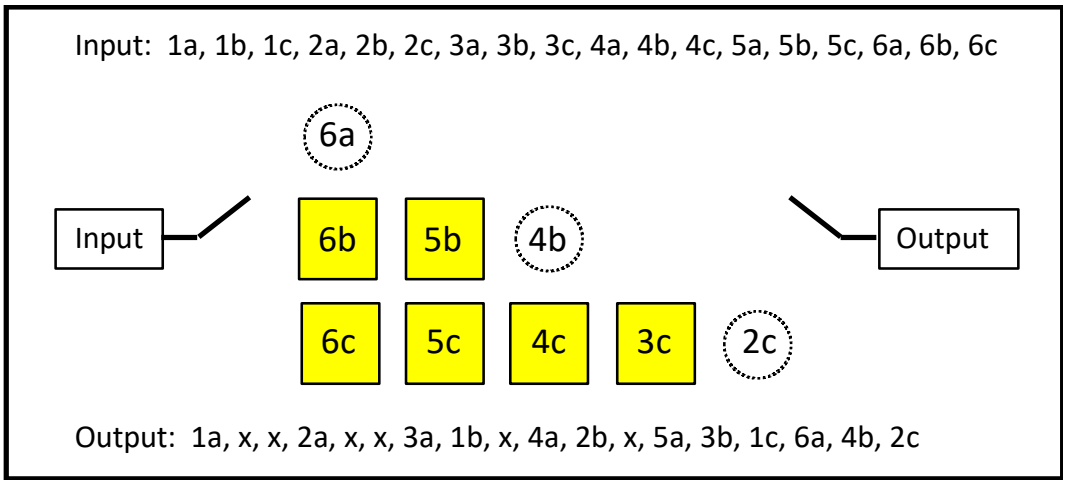
71. With reference to the third figure in the sequence below, input byte 3a is immediately output, then input byte 3b is stored in the interleaver memory, and

then input byte 3c is stored in the interleaver memory. Input byte 1b, which had been stored in the interleaver memory, is output following byte 3b.

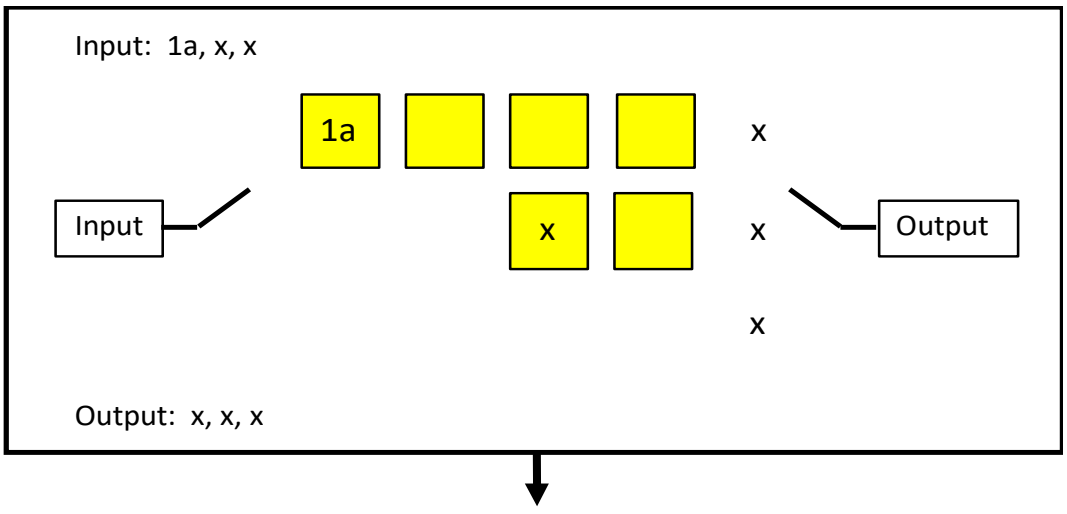


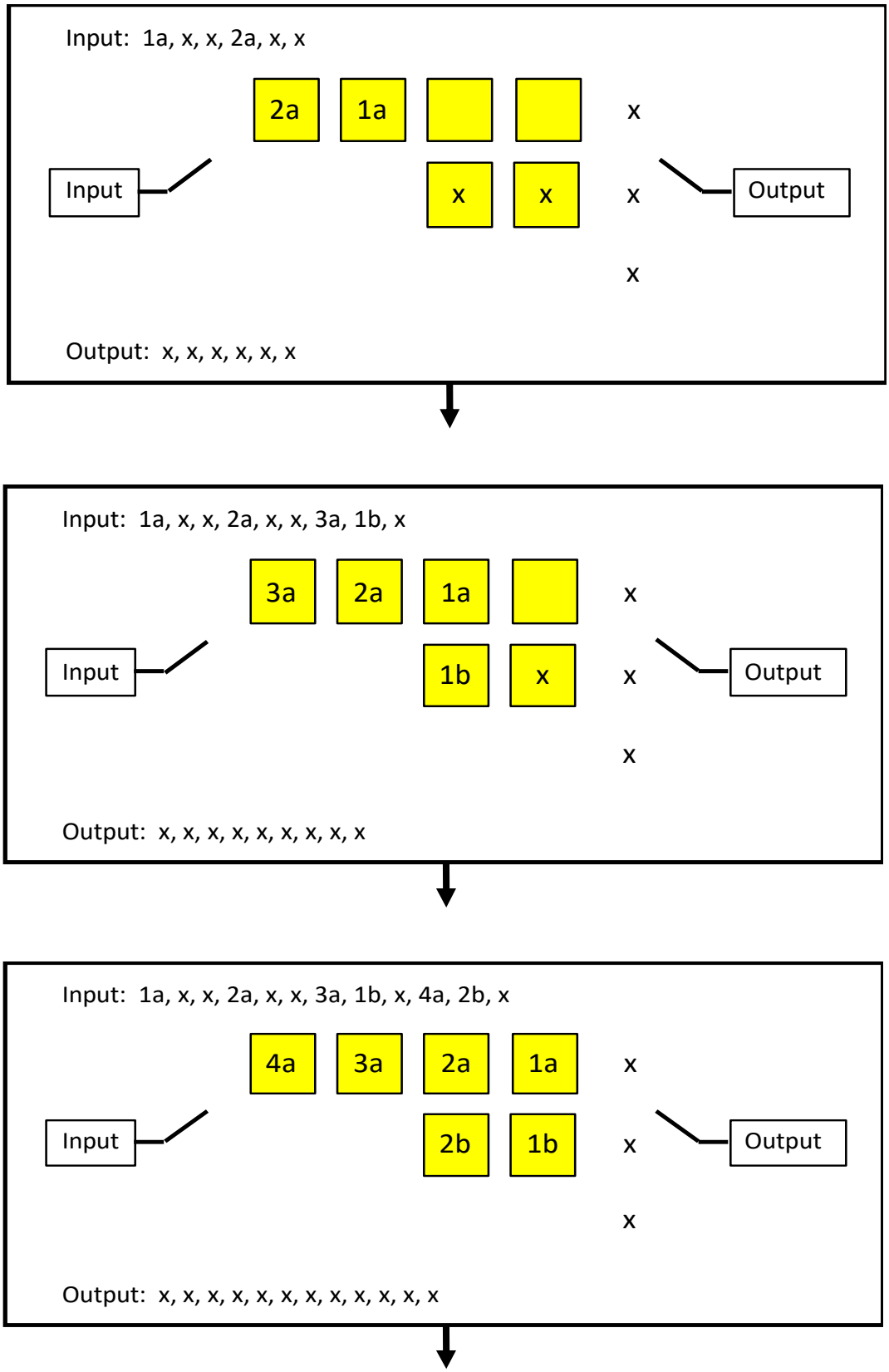
72. With reference to the fourth, fifth and sixth figures in the sequence below, the first byte of each block is output immediately without being stored in the interleaver memory. The second byte of each block is temporarily stored in the interleaver memory and then output such that it is seven byte positions away from the first byte of its respective input block. The third byte of each block is temporarily stored in the interleaver memory and then output such that it is seven byte positions away from the second byte of its respective input block.

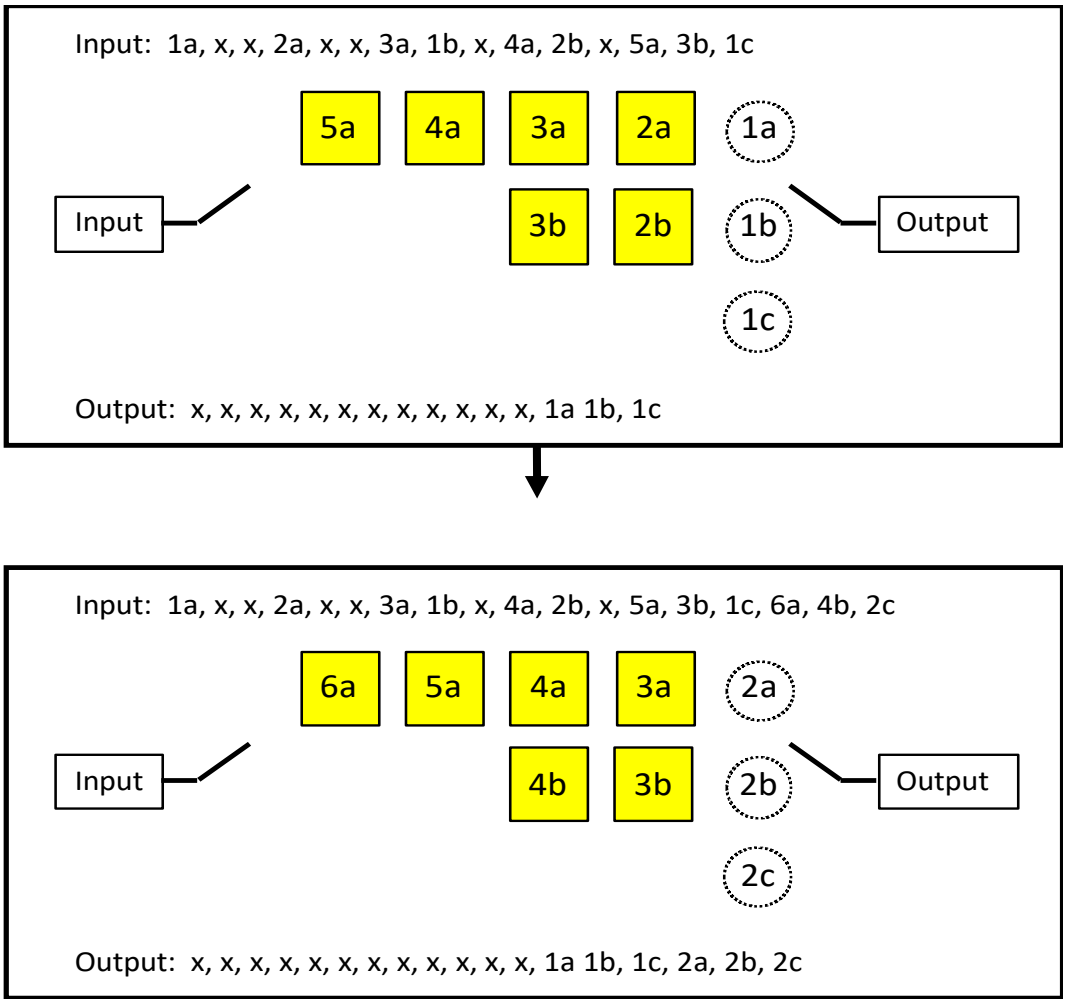

Input: 1a, 1b, 1c, 2a, 2b, 2c, 3a, 3b, 3c, 4a, 4b, 4c
4a
Input
4b
3b
2b
Output
4c
3c
2c
1c
x
Output: 1a, x, x, 2a, x, x, 3a, 1b, x, 4a, 2b, x
Input: 1a, 1b, 1c, 2a, 2b, 2c, 3a, 3b, 3c, 4a, 4b, 4c, 5a, 5b, 5c
5a
Input
5b
4b
3b
Output
5c
4c
3c
2c
1c
Output: 1a, x, x, 2a, x, x, 3a, 1b, x, 4a, 2b, x, 5a, 3b, 1c



73. A convolutional deinterleaver is essentially a mirror image of the interleaver. The following sequence of six figures shows deinterleaving of the interleaved byte stream that was output from the interleaver described above. The interleaved byte stream is input to the deinterleaver and the original byte stream is output with the original byte order. Note that the first 12 output bytes will be null bytes or bytes from earlier-received blocks. These 12 output bytes also are illustrative of the end-to-end delay (latency) associated with interleaving and deinterleaving.




Input: 1a, x, x, 2a, x, x
2a
1a
x
x
x
Input
Output
Output: x, x, x, x, x, x
Input: 1a, x, x, 2a, x, x, 3a, 1b, x
3a
2a
1a
1b
x
x
x
x
Input
Output
Output: x, x, x, x, x, x, x, x, x
Input: 1a, x, x, 2a, x, x, 3a, 1b, x, 4a, 2b, x
4a
3a
2a
1a
2b
1b
x
x
x
Input
Output
Output: x, x, x, x, x, x, x, x, x, x, x, x



74. The amount of interleaver and deinterleaver memory required at each transceiver is $\frac{\text{MAXDELAYOCTET}}{2}$. *Id.* ("The minimum amount of memory required in a transceiver (VTU-O or VTU-R) to meet this requirement is $\frac{\text{MAXDELAYOCTET}}{2}$ octets."). MAXDELAYOCTET is equal to the summation over all latency paths of the aggregate interleaver and deinterleaver delays, which is written as:

$$\sum_p \left(I_{\text{US},p} - 1\right) \times \left(D_{\text{US},p} - 1\right) + \left(I_{\text{DS},p} - 1\right) \times \left(D_{\text{DS},p} - 1\right). \; \textit{Id.}$$